

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

5 Listing of Claims:

Claim 1 (currently amended): A computer system comprising:

a transformer module having a first and second parallel port and a first and second serial port; and

a control unit capable of electrically disconnecting the first parallel port from the

10 first and the second serial ports and electrically connecting the first parallel port to the second parallel port. ~~- a first processor; a first serial/parallel data transformer comprising a parallel port and a serial port; a second serial/parallel data transformer comprising a parallel port and a serial port; and a control unit for selectively connecting in an electrical fashion the first processor to the parallel port of the first serial/parallel data transformer, the first processor to both the parallel port of the first serial/parallel data transformer and the parallel port of the second serial/parallel data transformer, or the first processor to the serial port of the first serial/parallel data transformer; and electrically connecting the serial port of the first serial/parallel data transformer to the serial port of the second serial/parallel data transformer.~~

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Claim 2 (currently amended): The computer system of claim 1 further comprising a first processor serial device electrically connected to the first parallel serial port of the 25 first serial/parallel data.

Claim 3 (currently amended): The computer system of claim 1 further comprising two serial devices respectively electrically connected to the serial port of the wherein the

transformer module further comprises a first serial/parallel data transformer electrically connected to the first parallel port and the serial port of the a second serial/parallel data transformer electrically connected to the second parallel port.

- 5 Claim 4 (currently amended): The computer system of claim [[1]] 2 further comprising a second processor electrically connected to the second parallel port of the second-serial/parallel data transformer.

10 Claim 5 (original): The computer system of claim 4 wherein the first processor has an operational voltage equal to that of the second processor.

Claim 6 (original): The computer system of claim 4 wherein the first processor has an operational voltage different from that of the second processor.

- 15 Claim 7 (currently amended): The computer system of claim [[1]] 3 further comprising a level shifter electrically connected between [[the]] a serial port of the first serial/parallel data transformer and [[the]] a serial port of the second serial/parallel data transformer for adjusting the level of data transmitted between the serial port of the first serial/parallel data transformer and the serial port of the second serial/parallel data transformer.

20 Claim 8 (original): The computer system of claim 1 wherein the control unit is a logic circuit.

- 25 Claim 9 (original): The computer system of claim 1 wherein the control unit is a program code stored in a memory.

Claim 10 (currently amended): The computer system of claim [[1]] 3 wherein the first serial/parallel data transformer, the second serial/parallel data transformer, and the

control unit are integrated on an application specific integrated circuit (ASIC).

Claim 11 (currently amended): The computer system of claim [[1]] 3 wherein the first serial/parallel data transformer is a universal asynchronous receiver/transmitter
5 (UART).

Claim 12 (currently amended): The computer system of claim [[1]] 3 wherein the first serial/parallel data transformer is an inter-IC (I.sup.2C).
10 Claim 13 (currently amended): The computer system of claim [[1]] 3 wherein the first serial/parallel data transformer is a universal serial bus (USB).

Claim 14 (currently amended): The computer system of claim [[1]] 3 wherein the first serial/parallel data transformer is a Serial Peripheral Interface (SPI).
15 Claim 15 (currently amended): The computer system of claim [[1]] 3 wherein the first serial/parallel data transformer is a Synchronous Serial Protocol interface (SSP).

Claim 16 (currently amended): The computer system of claim [[1]] 3 wherein the first
20 serial/parallel data transformer is a Microwire interface.

Claim 17 (currently amended): The computer system of claim [[1]] 3 wherein the first serial/parallel data transformer is an Inter IC Sound interface (I.sup.2S).
25 Claim 18 (currently amended): A serial/parallel data transformer module comprising:
a first serial/parallel data transformer comprising a parallel port and a serial port;
a second serial/parallel data transformer comprising a parallel port and a serial port;
and
a control unit for selectively selecting between a first state connecting in an

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electrical fashion the parallel port of the first serial/parallel data transformer to the parallel port of the second serial/ parallel data transformer while electrically disconnecting the first and the second serial ports [[or]] and a second state electrically connecting the serial port of the first serial/parallel data transformer to the serial port of the second serial/parallel data.

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Claim 19 (original): The serial/parallel data transformer module of claim 18 further comprising a level shifter electrically connected between the serial port of the first serial/parallel data transformer and the serial port of the second serial/parallel data transformer for adjusting the level of data transmitted between the serial port of the first serial/parallel data transformer and the serial port of the second serial/parallel data transformer.

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Claim 20 (original): The serial/parallel data transformer module of claim 18 wherein the control unit is a logic circuit.

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Claim 21 (original): The serial/parallel data transformer module of claim 18 wherein the control unit is a program code stored in a memory.

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Claim 22 (original): The serial/parallel data transformer module of claim 18 wherein the first serial/parallel data transformer, the second serial/parallel data transformer, and the control unit are integrated on an ASIC.

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Claim 23 (original): The serial/parallel data transformer module of claim 18 wherein the first serial/parallel data transformer is a UART.

Claim 24 (original): The serial/parallel data transformer module of claim 18 wherein the first serial/parallel data transformer is an I.sup.2C.

Claim 25 (original): The serial/parallel data transformer module of claim 18 wherein the first serial/parallel data transformer is a USB.

5 Claim 26 (original): The serial/parallel data transformer module of claim 18 wherein the first serial/parallel data transformer is a SPI.

Claim 27 (original): The serial/parallel data transformer module of claim 18 wherein the first serial/parallel data transformer is a SSP.

10 Claim 28 (original): The serial/parallel data transformer module of claim 18 wherein the first serial/parallel data transformer is a Microwire.

Claim 29 (original): The serial/parallel data transformer module of claim 18 wherein the first serial/parallel data transformer is an I.sup.2S.

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Claim 30 (new): A computer system comprising:

a first processor;

a first serial/parallel data transformer comprising a parallel port and a serial port;

20 a second serial/parallel data transformer comprising a parallel port and a serial port;

a second processor electrically connected to the parallel port of the second serial/parallel data transformer; and

25 a control unit for selectively connecting in an electrical fashion the first processor to the parallel port of the first serial/parallel data transformer, the first processor to both the parallel port of the first serial/parallel data transformer and the parallel port of the second serial/parallel data transformer, or the first processor to the serial port of the first serial/parallel data transformer; and

electrically connecting the serial port of the first serial/parallel data transformer to the serial port of the second serial/parallel data transformer.

Claim 31 (new): The computer system of claim 30 further comprising a serial device electrically connected to the serial port of the first serial/parallel data transformer.

5 **Claim 32 (new): The computer system of claim 30 further comprising two serial devices respectively electrically connected to the serial port of the first serial/parallel data transformer and the serial port of the second serial/parallel data transformer.**

10 **Claim 33 (new): The computer system of claim 30 further comprising a level shifter electrically connected between the serial port of the first serial/parallel data transformer and the serial port of the second serial/parallel data transformer for adjusting the level of data transmitted between the serial port of the first serial/parallel data transformer and the serial port of the second serial/parallel data transformer.**

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